

# Enhanced quantum efficiency of high-purity silicon imaging detectors by ultralow temperature surface modification using Sb doping

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A low temperature process for Sb doping of silicon has been developed as a backsurface treatment for high-purity *n*-type imaging detectors. Molecular beam epitaxy (MBE) is used to achieve very high dopant incorporation in a thin, surface-confined layer. The growth temperature is kept below 450 °C for compatibility with Al-metallized devices. Imaging with MBE-modified  $1k \times 1k$  charge coupled devices (CCDs) operated in full depletion has been demonstrated. Dark current is comparable to the state-of-the-art process, which requires a high temperature step. Quantum efficiency is improved, especially in the UV, for thin doped layers placed closer to the backsurface. Near 100% internal quantum efficiency has been demonstrated in the ultraviolet for a CCD with a 1.5 nm silicon cap layer. © 2005 American Institute of Physics. [DOI: 10.1063/1.2149181]

The next generation of astronomical missions will require instruments with the largest arrays of scientific imaging detectors ever flown in space, operating at extremely low light levels with stringent requirements for quantum efficiency (QE), optical bandwidth, and dark current ( $<10 \text{ e}^-/\text{pixel}/\text{h}$ ). The SuperNova acceleration probe led by Lawrence Berkeley National Laboratory (LBNL) is addressing these requirements by using a large array of high purity silicon charge coupled devices (CCDs). In order to achieve high QE and broadband response, conventional CCDs use a backilluminated configuration, in which the substrate is chemically and/or mechanically removed. Use of standard low-resistivity silicon limits the active detector thickness to 20  $\mu\text{m}$  or less, reducing the detector response at long wavelengths, where absorption takes place deeper in the silicon. By fabricating CCDs on high purity, *n*-type substrates (with impurity levels  $<10^{12} \text{ cm}^{-3}$ ) the active layer thickness can be increased to more than 250  $\mu\text{m}$ , enabling a strong near infrared to visible response.<sup>1</sup> Full depletion of these imagers also greatly improves the point spread function for high resolution imaging.<sup>2</sup>

High purity CCDs require a backsurface electrode that satisfies two conditions for optimal performance. First, absorption by the electrode must be minimized. The backsurface electrode plays an essential role in determining short wavelength (e.g., UV) QE because light in this spectral range is absorbed very close to the silicon surface. Second, the silicon surface must be passivated to minimize surface-generated dark current. The backsurface molecular beam epitaxy (MBE) growth process developed in this work fulfills these requirements in order to broaden the useful spectral range of high-purity silicon imagers, and provide high QE, low dark current, and long-term stability at a low cost.

We have previously demonstrated the effectiveness of backsurface electrodes formed by MBE growth of boron-doped silicon on thinned *p*-type (*n*-channel) CCDs.<sup>3</sup> Boron surface segregation is minimal and very sharply peaked ( $\delta$ -doped) layers can be grown within 1.5 nm of the backsurface. 100% internal quantum efficiency has been achieved with these CCDs in the UV, and detection of electrons directly impinging on CCDs has been demonstrated for energies as low as 50 eV.<sup>4</sup> In order to make this process widely applicable and cost effective for a variety of imagers, the MBE process is conducted at low substrate temperatures for compatibility with fully processed and metallized devices.

For low-light-level scientific imaging, *p*-channel CCDs fabricated on high purity *n*-type substrates are preferable to conventional *n*-channel CCDs, primarily because *p*-channel CCDs are less susceptible to bulk radiation damage.<sup>5,6</sup> Therefore, we have developed an MBE growth process using antimony as an *n*-type dopant for formation of a backsurface electrodes on *p*-channel CCDs. This process allows Sb delta layers to be deposited entirely at low temperature ( $<450 \text{ }^\circ\text{C}$ ). A complete description of our surface treatment and MBE growth process is given elsewhere.<sup>7</sup> In this work, silicon is supplied by an electron-beam source at a deposition rate of 0.04 nm/s, and Sb is supplied by a Knudsen cell heated to  $\sim 320 \text{ }^\circ\text{C}$  with a flux of  $\sim 1.5 \times 10^{12} \text{ cm}^{-2} \text{ s}^{-1}$ . A silicon buffer layer is deposited at 450 °C. The substrate is then cooled to 300 °C and  $\sim 0.4 \text{ ML}$  Sb is deposited followed by a silicon cap deposited at a rate of 0.04 nm/s.

The Sb doping process was applied to both photodiode test structures and  $1k \times 1k$  CCDs fabricated at LBNL and DALSA Semiconductor. Details about the structure and fabrication of these devices are described elsewhere.<sup>8,9</sup> An *in situ* reflection high-energy electron diffraction (RHEED) pattern of a Sb-doped CCD backsurface shows that after the growth is complete,  $2 \times 1$  surface reconstruction is still present, indicative of high quality crystalline material [see Fig. 1(a)]. Although Sb tends to surface segregate during

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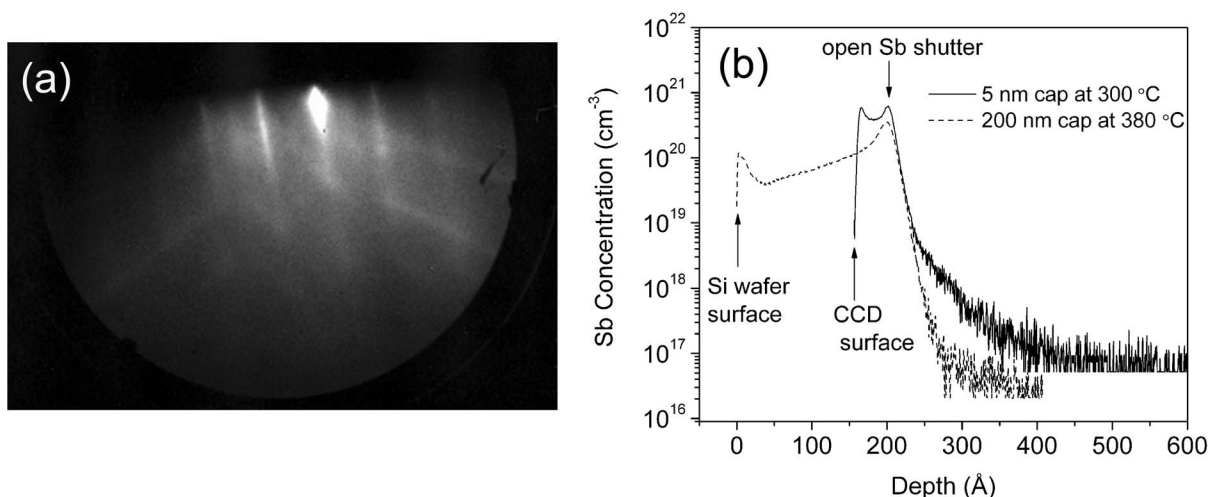


FIG. 1. (a) RHEED pattern and (b) SIMS of Sb doped layer grown at 300 °C with a 5 nm cap on a high purity  $1k \times 1k$  silicon CCD. For comparison, a profile for a higher temperature growth at 380 °C on a silicon wafer is shown. Surface segregation on the CCD is comparatively small. The total Sb dose measured by SIMS is  $2.5 \times 10^{14} \text{ cm}^{-2}$  for the CCD and  $2.3 \times 10^{14} \text{ cm}^{-2}$  for the 380 °C growth. Quadrupole SIMS analysis was performed by Charles Evans and Associates using a 500 eV Cs<sup>+</sup> ion beam impinging on the sample at an angle of 60°.

growth (to a larger extent than boron, for example), the full width at half maximum of the Sb concentration on a backside-treated CCD as measured by secondary ion mass spectroscopy (SIMS) is only 4.5 nm as shown in Fig. 1(b). Due to the high concentration of Sb throughout the layer, it is expected that it will make a sufficient backside contact even if the cap layer is thinner than 4.5 nm.

Hall effect measurements in conjunction with SIMS were used to determine the electrical activation of the Sb in MBE layers grown on high-purity silicon substrates. For example, after deposition of  $\sim 0.4$  ML of Sb and a 15 nm Si cap, the measured activated dose is  $\sim 2 \times 10^{14} \text{ cm}^{-2}$  which is  $\sim 85\%$  of the deposited dose. However, the conductivity of the Sb layer measured with the Hall probe decreases with decreasing silicon cap thickness (see Fig. 2). This decrease in conductivity is partially accounted for by Sb surface segregation during growth. Further reduction in conductivity may be accounted for by a reduction of the amount of Sb that is incorporated in substitutional sites due to near-surface defects.<sup>10</sup> Finally, the charge distribution in the vicinity of activated Sb might be altered by proximity to the surface.<sup>11</sup>

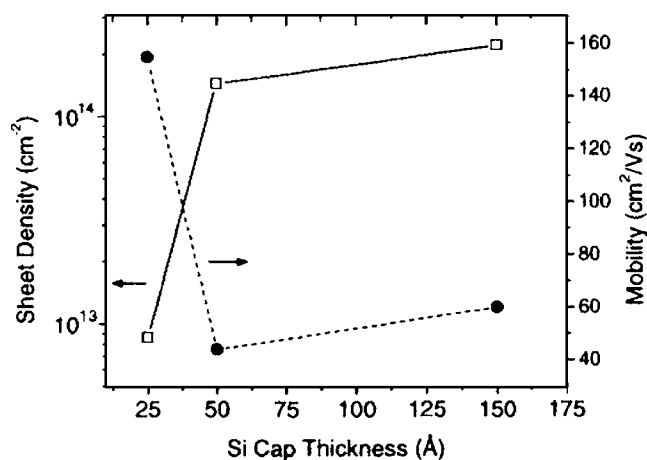


FIG. 2. Electron sheet density and mobility with increasing Si cap thickness obtained from Hall effect measurements using the Van der Pauw configuration with indium contacts and a field strength of 0.2 T. Sheet density is reproducible to within 3%, and mobility is reproducible to within 2%.

Photodiode test structures were used initially to test depletion width and dark current. Full depletion was observed at  $\sim 20$  V with a room temperature dark current of  $< 1 \text{ nA/cm}^2$  at 80 V, comparable to diodes with doped polysilicon backcontacts (a process that is incompatible with low temperature growth on fully processed devices).

Full compatibility of the Sb-doping process with  $1k \times 1k$  CCDs operated in full depletion has been demonstrated. A test pattern image is shown in Fig. 3 and QE data are shown in Fig. 4 for CCDs with  $\sim 3 \times 10^{14} \text{ cm}^{-2}$  Sb and different Si cap thicknesses, 1.5, 2.5, 5.0, and 15.0 nm. Some deviation from the reflection-limited response is observed. For example, the QE is lower than expected at 350 and 450 nm and higher at 900 nm. These deviations are attributed to systematic errors in the measurement setup resulting from several factors, including low source intensity in the 300–400 nm range, a low-intensity red leak, the use of filters for spectral discrimination, and inherent differences in the spectral response of the reference diode and the CCD. However, a clear trend of increasing QE with thinner cap layers is

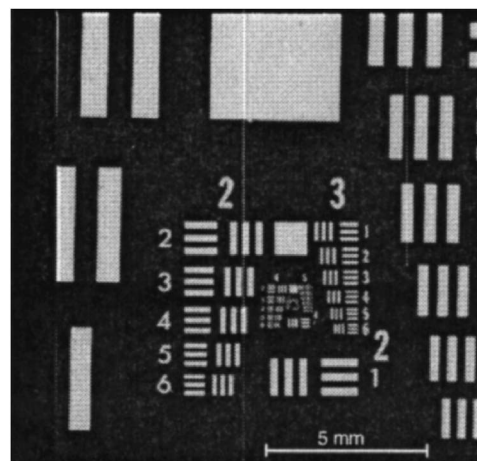


FIG. 3. (a) Test pattern image taken on 250- $\mu\text{m}$ -thick, backilluminated,  $1230 \times 1170$ ,  $12 \mu\text{m}$  pixel LBNL CCD at  $-140$  °C, with backside Sb doping by MBE and a 15 nm Si cap layer. The substrate bias of 45 V was sufficient to fully deplete the CCD. A vertical short unrelated to the MBE process is visible down the center of the image.

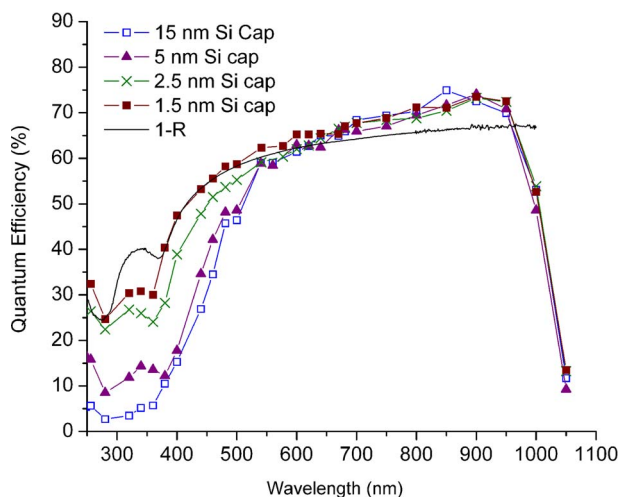


FIG. 4. (Color online) Quantum efficiency of CCDs with 1.5, 2.5, 5.0, and 15.0 nm Si cap layers measured at  $-100^{\circ}\text{C}$ . Measured 1-R indicates the maximum external QE that can be attained due to reflection from the silicon surface. It should be noted that these CCDs do not have antireflective coatings. QE in the red ( $>650\text{ nm}$ ) appears higher than the expected reflection-limited QE ( $\sim 65\%$ ), but this can be attributed to the poor response of the calibration diode in this region. Due to measurement noise present for the 2.5 and 5.0 nm devices, an accurate value of  $e^{-}/\text{DN}$  could not be established leading to a gain offset. Therefore, these curves have been adjusted to line up with the other curves in the long wave region. Adjustments were approximately 10%.

observed, especially in the UV region where significant absorption occurs *within* the MBE layer. For the 1.5 nm cap layer, near 100% internal quantum efficiency has been achieved over the entire spectral range from 250 to 900 nm. Room temperature dark current measured in diode mode was  $\sim 4\text{ nA}/\text{cm}^2$  at 50 V which is within normal range for these CCDs. The lowest dark current was  $0.5\text{ e}^{-}/\text{pixel}/\text{h}$ , measured at 138 K in a CCD with  $9\text{ }\mu\text{m}$  pixels and a MBE cap layer 2.5 nm in thickness. The dark current was observed to increase to  $7\text{ e}^{-}/\text{pixel}/\text{h}$  for a  $15\text{ }\mu\text{m}$  pixel device for the thinnest cap layer tested (1.5 nm). When normalized to pixel area this increase is a factor of approximately 5 as the cap layer thickness is decreased from 2.5 to 1.5 nm. It should be noted that this is still well within the operable range. While these numbers are suggestive that we may be approaching the lower useful limit on cap layer thickness achievable by this process, more work is underway to determine whether

the observed increase in dark current for the 1.5 nm cap layer is statistically significant. It should also be noted that devices with 2.5 nm cap layers were comparable in dark current to those with thicker cap layers. This is an indication that the activated Sb layer is sufficient to create a functional back electrode, despite the observed lower concentration observed by Hall effect.

Testing of photodiodes and CCDs with MBE-grown Sb layers indicates that we can form a thin low-temperature backsurface contact with low dark current. Enhanced short-wavelength QE was observed for Sb layers grown closer to the surface, with nearly 100% internal QE achieved at wavelengths as low as 250 nm with a 1.5 nm Si cap layer.

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